REMARKS

Claims 1-20 were pending in this application.

Claims 1-20 have been rejected.

No claims have been allowed.

Claims 1-20 remain pending in this application.

Reconsideration of Claims 1-20 is respectfully requested.

I. AMENDMENTS TO THE SPECIFICATION

The text of the specification has been amended to correct typographical errors. No new matter has been added to the specification as a result of the amendments.

II. REJECTIONS UNDER 35 U.S.C. § 112

The January 11, 2008 Office Action rejected Claims 1-20 under 35 U.S.C. § 112, first paragraph, for supposedly failing to comply with the written description requirement. The Examiner stated that the subject matter "a block based memory allocation unit" was not described in the specification. (January 11, 2008 Office Action, Page 2, Paragraph 3). The Applicants respectfully traverse this assertion of the Examiner.

The specification of the patent application does describe a block based memory allocation unit that allocates memory blocks to at least one hash table. The network packet search engine (NPSE) 102 of the present invention forms a block based memory allocation unit that allocates memory blocks to at least one hash table. "In the present invention, NPSE 102 performs the

IP lookup using, to the extent possible, a hash table in on-chip SRAM memory 107." (Specification, Paragraph [0018], Page 11, Lines 3-5). "In the present invention, an on-chip SRAM 107 holds hash tables 109 created by and accessed using at least one hash function 108, with an overflow CAM 103 to handle collisions. To minimize collisions, utilization of SRAM 107 is maximized by an on-demand block-based allocation scheme to make efficient use of available memory resources and rehashing." (Specification, Paragraph [0024], Page 14, Lines 1-7) (Emphasis added).

The network packet search engine (NPSE) 102 of the present invention minimizes collisions by using a block-based SRAM memory allocation for each hash table. "A second optimization to minimize collisions in the present invention is use of block-based SRAM allocation for each hash table. A small, fixed block of SRAM is first allocated for a given hash table. When rehashing no longer yields an empty slot (i.e., the existing block is full), another block is allocated and the IP address is hashed into the second block. This on-demand block allocation makes efficient use of available SRAM while minimizing collisions." (Specification, Paragraph [0027], Page 15, Line 22 to Page 16, Line 6). The specification clearly shows that the network packet search engine (NPSE) 102 of the present invention is a block based memory allocation unit that allocates memory blocks to at least one hash table.

Therefore, the Applicants respectfully submit that Claims 1-20 do comply with the written description requirement and respectfully request that the rejections of Claims 1-20 under 35 U.S.C. § 112, first paragraph, be withdrawn.

The January 11, 2008 Office Action also rejected Claim 3 and Claim 16 under 35 U.S.C. § 112, second paragraph, for supposedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner stated that it is not clear what is meant by "a selected limited number of memory blocks". (January 11, 2008 Office Action, Page 3, Paragraph 5). The Applicants respectfully traverse this assertion of the Examiner.

The specification of the patent application makes it clear what is meant by the term "a selected limited number of memory blocks." The specification states "Different criteria may be set for determining when to stop allocation blocks to a given has table, the simplest of which is to pre-assign a fixed (maximum) number of blocks n and stop when all of those blocks are allocated to the hash table, an approach reducing design risks." (Specification, Paragraph [0028], Page 16, Lines 17-22). The fixed (maximum) number of blocks "n" is also shown in FIGURE 3. In view of this description it is clear that the selected limited number of memory blocks that is referred to in Claim 3 and in Claim 16 is the pre-assigned (i.e., "selected") limited number (fixed maximum number "n") of memory blocks. The specification makes the meaning clear.

Therefore, the Applicants respectfully submit that Claim 3 and Claim 16 are not indefinite and respectfully request that the rejections of Claim 3 and Claim 16 under 35 U.S.C. § 112, second paragraph, be withdrawn.

III. REJECTIONS UNDER 35 U.S.C. § 102

The January 11, 2008 Office Action rejected Claims 1-3, 5-16 and 18-20 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,665,297 to Hariguchi et al. (hereafter "*Hariguchi*"). The Applicants respectfully traverse these rejections.

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

Independent Claims 1, 10 and 14 claim an address lookup structure that comprises a block based hashing lookup search mechanism. The block based hashing lookup search mechanism comprises a routing table implemented with selective hashing for a plurality of prefixes with different lengths and a block based memory allocation unit that allocates memory blocks to said at least one hash table.

The block based hashing lookup search mechanism of the Applicants' invention is not shown in the *Hariguchi* reference. In particular, the block based memory allocation unit that allocates memory blocks to at least one hash table is not shown in the *Hariguchi* reference. The Examiner stated that the hash bucket 160 of the *Hariguchi* reference could be viewed as a unit for allocating memory for storing the route entries. (January 11, 2008 Office Action, Page 4, Lines 3-5). The Applicants respectfully traverse the statement of the Examiner that

the hash bucket 160 discloses or suggests a block based memory allocation unit of the type disclosed and claimed by the Applicants. The hash bucket 160 of the *Hariguchi* reference stores network addresses and output pointers at addresses corresponding to the hash value of their associated masked destination addresses. (*Hariguchi*, Column 6, Line 66 to Column 7, Line 2). There is no mention in the *Hariguchi* reference of memory blocks or of a mechanism for allocating memory blocks. The *Hariguchi* reference does not disclose or suggest a block based memory allocation unit of the type disclosed and claimed by the Applicants.

Therefore, Claims 1-3, 5-16 and 18-20 are not anticipated by the *Hariguchi* reference. Accordingly, the Applicants respectfully request withdrawal of the § 102 rejections and full allowance of Claims 1-3, 5-16 and 18-20.

IV. REJECTIONS UNDER 35 U.S.C. § 103

The January 11, 2008 Office Action rejected Claim 4 and Claim 17 under 35 U.S.C. § 103(a) as being unpatentable over *Hariguchi* in view of U.S. Patent No. 6,625,612 to Tal et al. (hereafter "*Tal*"). The Applicants respectfully traverse these rejections.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 USPQ2d 1780, 1783 (Fed. Cir.1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of

obviousness is established does the burden shift to the Applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed.Cir.1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir.1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the Applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 USPQ.870, 873 (Fed.Cir.1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed.Cir.1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on the Applicant's disclosure. MPEP § 2142.

The Applicants herein incorporate by reference the arguments and remarks previously made with respect to the anticipation rejections of Claims 1-3, 5-16 and 18-20.

As previously shown, Claim 1 is patentable. As a result, Claim 4 is also patentable due to its dependence from Claim 1. The Examiner stated that the *Hariguchi* reference does not disclose a second of two hash functions employed when a collision occurs with a first of the two

has functions. (January 11, 2008 Office Action, Page 7, Paragraph 9). The Applicants agree that the *Hariguchi* reference does not show this element of the Applicants' invention. The *Tal* reference does not supply the deficiencies of the *Hariguchi* reference. There is nothing in the *Hariguchi* reference or in the *Tal* reference that shows the elements of Claim 1 or Claim 4.

As previously shown, Claim 14 is patentable. As a result, Claim 17 is also patentable due to its dependence from Claim 14. The Examiner stated that the *Hariguchi* reference does not disclose a second of two hash functions employed when a collision occurs with a first of the two has functions. (January 11, 2008 Office Action, Page 7, Paragraph 9). The Applicants agree that the *Hariguchi* reference does not show this element of the Applicants' invention. The *Tal* reference does not supply the deficiencies of the *Hariguchi* reference. There is nothing in the *Hariguchi* reference or in the *Tal* reference that shows the elements of Claim 14 or Claim 17.

The proposed combination of the *Hariguchi* reference and the *Tal* reference fails to disclose, teach, or suggest all elements of Claim 1 (and Claim 4) and Claim 14 (and Claim 17). Accordingly, the Applicants respectfully request withdrawal of the § 103 rejections of Claim 4 and Claim 17 and full allowance of Claims 1-20.

V. CONCLUSION

The Applicants respectfully assert that all pending claims in this application are in condition for allowance and respectfully request full allowance of Claims 1-20.

SUMMARY

The Applicants respectfully assert that all pending claims in this application are in condition for allowance and respectfully request full allowance of the claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@munckbutrus.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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